REMARKS

In response to the Office Action mailed July 22, 2004, Applicant respectfully requests reconsideration.

Preliminarily, Applicant notes with appreciation the indication of allowable subject matter in claims 14 and 15.

The Office Action objected to the title of the application as being in conflict with co-pending application serial number 09/981,624. In view of the fact that the title in the co-pending application has been changed, this objection should now be moot and Applicant respectfully requests that the objection be withdrawn.

Claims 1, 3, 8, 9, and 11 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 3 of co-pending patent application serial number 09/981,624. Although Applicant respectfully disagrees with this rejection and believes that the claims of the co-pending application are patentably distinct from each other, for purposes of expediting prosecution, Applicant files herewith a Terminal Disclaimer with respect to co-pending application serial number 09/981,624. Accordingly, the double patenting rejection is overcome and Applicant respectfully requests that the rejection withdrawn.

Minor clarifying amendments that do not narrow the scope have been made to claim 1.

Claims 1-13 were rejected under 35 U.S.C. §102(e) as being anticipated by Swoboda (U.S. Patent Application Publication No. US2002/0059541). Applicant respectfully traverses this rejection.

Swoboda is directed to automatic detection of connectivity between an emulator and a target device. FIG. 1 of Swoboda shows an emulation system including an emulation controller 12 connected to a target system 16 via a target cable (Swoboda [0081]). FIG. 2 illustrates the connections of an emulator such as shown in FIG. 1 and a plurality of target devices, in the diagram, integrated circuit chips. The connections illustrated in FIG. 2 also use cables (Swoboda [0082]).

In Swoboda, the emulation device is not placed on the integrated chip but connected to the integrated chip via cables (Swoboda [0081]), and is therefore a separate emulator unit. Swoboda includes an off-chip emulation device that provides on-chip debug facilities (Swoboda [0055]-[0060]). Swoboda also explains as chip integration levels increase, CPU clock rates are also increasing. Increased CPU clock rates result in on-chip subsystems to be operated at clock rates slower than the CPU clock. Therefore, a clear view of the CPU is unattainable under the on-chip subsystem method of operation (Swoboda [0016]).

By contrast, claim 1 recites an integrated circuit chip comprising an embedded digital processor and an on-chip emulation device coupled to said digital processor, said emulation device being operable to control said digital processor and to collect information about the operation of said digital processor, the on-chip emulation device having a communication port for off-chip communication, the chip further comprising an on-chip interface having a first port connected to said communication port of said on-chip emulation device and a second port for connection to a non-proprietary bus wherein said interface is operable to convert between a format suitable for said on-chip emulation device and a format suitable for said non-proprietary bus.

Clearly, Swoboda does not teach or suggest an integrated circuit chip comprising an embedded digital processor and an on-chip emulation device coupled to the digital processor. Clearly, claim 1 distinguishes over Swoboda and is in allowable condition. Accordingly, Applicant respectfully requests that the rejection under 35 U.S.C. §102(e) with respect to claim 1 be withdrawn.

Claims 2-7 depend from claim 1 and are allowable for at least the same reasons.

Claim 8 recites a method of communicating between a remote device and a digital processor, said digital processor being on an integrated circuit chip, said chip having on-chip emulation circuitry for monitoring and controlling the digital processor in response to signals from a said remote device, said chip further comprising interface circuitry disposed between a port of said on-chip emulation circuitry and a communication port for said signals, wherein said port is adapted to receive a non-proprietary bus and wherein said non-proprietary bus is adapted to convey signals having a predetermined protocol, the method comprising connecting said non-

proprietary bus to said port and to a said remote device; receiving said signals from said remote device over said non-proprietary bus in said non-proprietary protocol at said communication port and transferring said signals to said interface circuitry on-chip; in said interface circuitry, converting said signals into a form suitable for said on-chip emulation circuitry, and transferring said converted signals to said on-chip emulation circuitry whereby said on-chip emulation circuitry responds to said converted signals to monitor and control said digital processor.

As discussed above in connection with claim 1, Swoboda does not teach or suggest digital processing circuitry and on-chip emulation circuitry for monitoring and controlling the digital processor. Claim 8 clearly distinguishes over Swoboda and is in allowable condition. Accordingly, Applicant respectfully requests that the rejection of claim 8 under 35 U.S.C. §102(e) be withdrawn.

Claims 10-15 depend from claim 8 and are allowable for at least the same reasons.

Claim 9 recites a method of debugging a digital processor using a host computer, said digital processor being on an integrated circuit chip, said chip having on-chip emulation circuitry for monitoring and controlling the digital processor in response to signals from said host computer, said chip further comprising interface circuitry disposed between a port of said on-chip emulation circuitry and a communication port for said signals, wherein said port is adapted to receive a non-proprietary bus and wherein said non-proprietary bus is adapted to convey signals having a predetermined protocol, the method comprising connecting said non-proprietary bus to said port and to a said host computer; generating said signals in said host computer; receiving said signals from said host computer over said non-proprietary bus in said non-proprietary protocol at said communication port and transferring said signals to said interface circuitry on-chip; in said interface circuitry, converting said signals into a form suitable for said on-chip emulation circuitry, and transferring said converted signal to said on-chip emulation circuitry whereby said on-chip emulation circuitry responds to said converted signals to monitor and control said digital processor.

As discussed above in connection with claim 1, Swoboda does not teach or suggest on-chip emulation circuitry for monitoring and controlling the digital processor. Clearly, claim 9

distinguishes over Swoboda and is in allowable condition. Accordingly, Applicant respectfully requests that the rejection of claim 9 under 35 U.S.C. §102(e) be withdrawn.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

Anthony DEBLING

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